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Patent
DB000575-015

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Keeth, et al.	**Examiner:**	
Serial No.:	09/899,977	**Art Unit:**	2818
Filed:	07/06/2001		

Entitled: 256 MEG DYNAMIC RANDOM ACCESS MEMORY

SECOND PRELIMINARY AMENDMENT

Preliminary to the examination of the above-identified application, please amend the claims as follows.

70. (Once Amended) A dynamic random access memory, comprising:

an array of memory cells[, each comprised of two storage elements];

a plurality of peripheral devices for writing data into said memory cells and for reading data out of said memory cells;

a plurality of voltage supplies responsive to an external voltage for generating a plurality of supply voltages for use by said array and said plurality of peripheral devices; and

test mode logic for determining whether the memory is in a test mode, and wherein said plurality of peripheral devices includes a [latch] latching circuit responsive to a first external signal when the memory is in the test mode, for latching data stored in a first seed group of memory elements, and [a write] an enable circuit responsive to a second external signal when said memory is in the test mode, for enabling the latched data to be written to a second group of memory elements.

71.(Once Amended) A method of testing a plurality of memory elements organized in a plurality of rows, comprising the steps of:

writing test data into a first seed row of memory elements;